# Modeling ASIC Memories in FPGA-Based Prototype Systems

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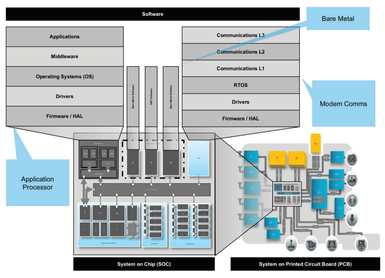
FROM CHIPS TO SYSTEMS – LEARN TODAY, CREATE TOMORROW

## System and Chip Design in 2019 and Beyond

- Time to market
- Development cost reduction
- Exponentially increasing embedded software contents
- **Memories (size, complexity, protocols)**
- Multi-core design and verification complexity

AND…

- Speed, speed, speed
  - To run SW, HW regressions, system validation



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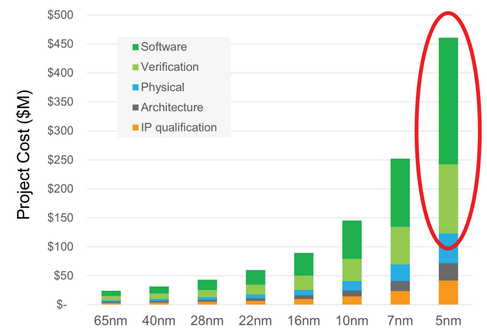
## Software Is the Biggest Challenge




*Source: IBS 2018*

**VERIFICATION and SOFTWARE**

$2^N$

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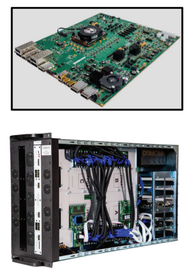
## And this Is Where FPGA-Based Prototyping Helps

- **Primary platform for pre-silicon software development and validation**
  - Maps a digital ASIC, ASSP, SoC design, or part thereof into one or more FPGAs
- **Allows software to execute in real-world environments**
  - Provides pre-silicon execution speeds in the 10s of MHz
  - Enables connectivity to real peripherals
    - Runs real-world traffic flows including interrupts and random events
    - Runs error conditions and handles errata with other system components



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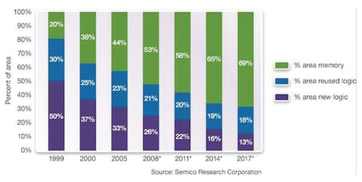
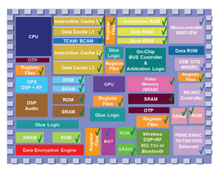
## Not So Fast, Though… SoC Design Contains **a Ton** of Memories

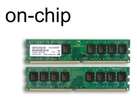
- By now, over 70% of the chip is memory
  - Cache memories
  - On-chip SRAM and ROM
  - FIFOs and buffers
  - Multi-port memories




Source: Semico Research Corporation




- Off-chip bulk memory needs on-chip memory controllers
  - LPDDR
  - HBM
  - UFS
  - FLASH
  - Etc



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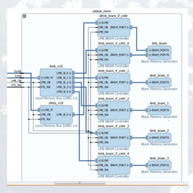
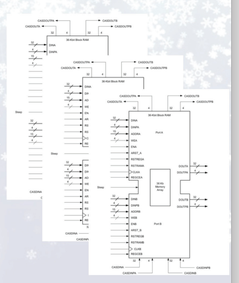
## Memories Are Like Snowflakes…

- All look alike, yet all are different
  - Many different types
  - Many different protocols
  - Any size, and # of read/write ports





Source: Xilinx

- Yet, FPGAs have only fixed-size, dual-port memories

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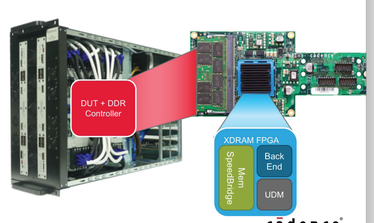
## So, What Now – How Do You Deal with That?

Use Cadence® Protium™ S1/X1 prototyping platforms for all FPGA-based prototyping

- Innovative memory solutions
  - Automatic memory compiler
  - Memory backdoor upload/download
  - Memory speed-bridge functionality
  - Comprehensive portfolio of memory models
  - XSRAM for any kind of memory up to 128MB
  - XDRAM for any kind of DDR-type memory



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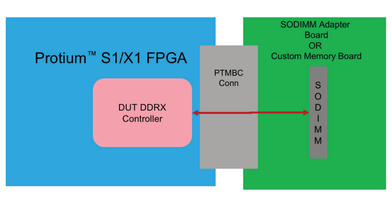
## Implementation Options – Directly Connected Memory

- Highest performance
  - Faster the FPGA is running, the easier it is to deploy
- Any memory / any size
  - May require custom board design
- Caution: Requires expert design knowledge and FW modifications!




***Steps to bring-up direct connect DDR interfaces***

1. FW code modification - Mode register changes
   - Switch off the DLL
   - Switch off ODT
   - Set CAS latency to only level supported (6) when DLL is disabled
2. Bypass write and read leveling
   - Need accurate modeling of delay cells in PHY
3. Modify read capture logic
   - CAS Latency changes in DLL bypass
   - Need to reduce DQ capture to CL-1 – *Can require design modifications*
4. Biggest issue – Refresh !
   - Need to run refresh out of spec, otherwise eats up bandwidth
   - Characterized data shows 2X-5X out of spec is acceptable
   - FW needs updated to adjust refresh counters in memory controller

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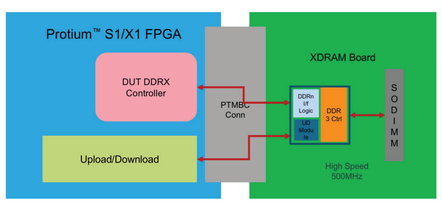
## Implementation Options – XDRAM

- Modeling approach based on Cadence® MMP IP
  - Supports LPDDR2/3/4, DDR3/4, HBM, UFS, etc
  - No change to design memory controller and firmware
  - Support for backdoor upload/download
  - Acts as memory SpeedBridge™ Adaptor (timing, refresh, etc.)




***Protium Benefits of XDRAM Solution***
- No DUT design modifications needed
- No changes to the FW or configuration
- DQS timing easily handled using compiler terminalTiming
- Adds runtime back-door for upload and download feature
- System data throughput not impacted by refresh issue

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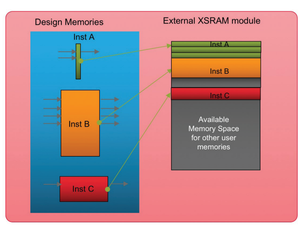
## Implementation Options – XSRAM

- Modeling approach based on Cadence® MMP IP
  - Up to 128MB capacity
  - Fully automatic
  - Sync memories up to 512bit wide
  - Multi-port and multi-instance per module




***Overall Benefits of External SRAM***
- Fast SRAM memories can operate at up to 200MHz
- Significantly more capacity than on FPGA memory resources

***Additional Protium™ S1/X1 platform advantages***
- Memory compiler can automatically change memory aspect ratio to fit real SRAMs shape – Supports 1-bit to 512-bit data widths
  - Can be achieved in a manual flow but time consuming
- Memory compiler can automatically stack multiple user memory instances
  - Very difficult to achieve manually, memories in different hierarchies, memories of different aspect ratios
- Memory compile optimizes scheduling of multiple design ports
  - Similar to FPGA memories, SRAM devices are typically only 2-port memories

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## Comprehensive, Automated Memory Support

The conversion and implementation of memories is one of the most challenging and time-consuming steps in the bring-up of an FPGA-based prototype system, often taking many weeks to complete

| Type | Size | MMP | Upload/ Download | Comments |
|---|---|---|---|---|
| FPGA-internal | ~50Mbits/FPGA | Yes | Yes | • Fully automatic compile<br>• Upload/download limited to 32 memory blocks max. per FPGA |
| XSRAM (automated small external memory) | 128Mbytes per memory card | Yes | Yes | • Fully automatic compile<br>• Extends 'FPGA-internal' memory to external SRAM<br>• Useful for SPI-flash and other small memories (e.g., boot ROM) |
| XDRAM (automated bulk memory) | 16GBytes per XDRAM card | Yes | Yes | • Semi-automatic compile<br>• Leverages XDRAM hardware support for DDR3/4, LPDDR3/4 |
| DCMC (Direct connected memory card) | x GBytes (depending on memories used) | No | No | • Design change may be required, depending on memory type<br>• App notes available |
| FCMC (Full-custom memory card) | Custom | No | No | • Full custom development |

 

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## Protium – The Most Efficient Way to Prototype Your ASIC

- Fast time-to-prototyping (days or week – not months)
  - No RTL changes
  - Multi-FPGA auto-partitioning / memory compilation / timing closure
  - Fully integrated FPGA place-and-route

- Scalable performance (up to 100MHz, and more)
  - From fully automatic to fully manual
  - Advanced black-box methodology

- Advanced software debug
  - Memory upload/download
  - Clock control start/stop
  - Signal force/release
  - Prototyping full visibility

 

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